# ETS'09 Technical Program

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## Monday, May, 25, 2009

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## TTEP Tutorial

9:00 – 13:00 and 14:30 – 17:30

**Tutorial**

**Advanced Topics and Recent Advances in Silicon Debug and Diagnosis**

Srikanth VENKATARAMAN, Intel Corp., USA, Miron ABRAMOVICI, Dafca Corp., USA, Robert AITKEN, ARM, USA

Summary: The increasing design complexity along with the emergence of new failure mechanisms in the nanometer regime has significantly increased the complexity of verification, validation and manufacturing ramp of ICs. When pre-silicon verification and validation uncovers design bugs, the process of diagnosing and debugging these issues is called design error diagnosis. From the time a new chip comes back from the fab until high-volume production can start, the chip goes through functional silicon validation and debug to make sure it is free of design errors, and defect diagnosis and failure analysis to solve yield problems. These activities, referred to as silicon debug and diagnosis, have become the most time-consuming phase in the development cycle of a new design, increasing to about 33% of the total time. This is a consequence of the increasing design complexity, along with the emergence of new failure mechanisms in nanometer technologies. Long time-to-volume and low manufacturing yield have a great detrimental impact on the economic viability and the overall success of a product. This tutorial covers the state of the art and the full spectrum of topics in silicon validation and debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques. We will also describe successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies. Finally we will discuss future directions and challenges.

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## Tuesday, May 26, 2009

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### 8:30 – 10:30 Session 1: **Plenary Opening**

*Moderator*: Bashir Al.Hashimi, Southampton Univ., UK

8:30 – 8:40 **Welcome Address**
Jose Luis Huertas, CNM, Spain – ETS'09 General Chair

8:40 – 8:50 **Technical Program Overview**
J. Paulo Teixeira, IST/INESC-ID, Portugal, ETS'09 Program Chair

8:50 – 9:00 **Presentation of ETS'08 Best Paper Award**
Patrick Girard, LIRMM, France – ETS'08 Program Chair

9:00 – 9:10 **TTTC Award Ceremony**
Yervant Zorian, Virage Logic, USA, TTTC Senior Past Chair

#### 09:10 – 09:50 **Keynote 1: We have got compression, what next?**

**Janusz Rajski**, Mentor Graphics Corp., USA

Abstract: Test compression is one of the fastest adopted DFT methodologies. It was commercially introduced eight years ago, and now it has become the mainstream DFT technology. Disruptive technology of this magnitude has impact that goes far beyond cost of manufacturing test. Test compression has changed competitive landscape, opened up completely new opportunities in product quality and yield management, and has redefined DFT technology roadmaps. It stimulates research and development activities in new areas that until now were considered not promising or not practical, enables quality of testing that was unachievable until now, accelerates adoption of new fault models that take into account physical data bases and timing information, and changes how fault diagnostics and yield learning are done in manufacturing environment.

There is a passionate debate in the professional community on the future of test compression. How scalable is it? How long will it keep up with the growing sizes of designs? What is the maximum achievable compression? How can we accommodate power constraints? What is its impact on our ability to perform diagnosis in volume production? Was it a one time deal or is it scalable solution that will be around for many generations of semiconductor technologies? Some voices focus on opportunities, others point to limitations. Some arguments are grounded in engineering others resort to financial analysis. Many of the predictions are conflicting. The presentation will discuss many of these issues, new opportunities, new and not so new challenges, as well as future technology roadmaps.

#### 09:50 – 10:30 **Keynote 2: Something I Always Wanted to Know About Test, But Was Afraid to Ask**

**Christian Landrault**, LIRMM, France

Abstract: As pinpointed in the last ITRS report and also clearly highlighted in the past years test conference programs, the overall mission of manufacturing test is continuously shifting from its "screening defects" basic and primary objective towards more subtle and secondary goals constituted for example by reliability aspect and yield learning. Just after his retirement, the author examines these new testing opportunity and will try to give directions to all what he missed and failed to do in his research career.

### 10:30 – 11:30 Session 2: **Poster Session I**

- **Testing of Strongly-Indicating Asynchronous Datapaths**

Deepali KOPPAD, University of Edinburgh, UK

- **A Methodology to Evaluate Transient-Fault Effects on Asynchronous and Synchronous Circuits**
  Rodrigo POSSAMAI BASTOS, TIMA, France, Yannick MONNET, TIEMPO, France, Gilles SICARD, Fernanda KASTENSMIDT, UFRGS, Brazil, Marc RENAUDIN, TIEMPO, France, Ricardo REIS, UFRGS, Brazil
- **On-line error detection of a compact 32 bit hardware AES implementation**
  Uros LEGAT, Anton BIASIZZO, Franc NOVAK, Jozef Stefan Institute, Slovenia
- **A High Precision Analog Signal Generator Design for ADC BIST**
  Vincent O BRIEN, Brendan MULLANE, Thomas FLEISCHMANN, C MACNAMEE, Univ. of Limerick, Ireland
- **Deterministic scan-chain diagnosis for intermittent faults**
  Dan ADOLFSSON, NXP Semiconductors, the Netherlands, Joanna SIEW, Philips Applied Technologies, the Netherlands, Erik LARSSON, Linkoping University, Sweden, Erik Jan MARINISSEN, IMEC, Belgium
- **A SBST Methodology for applying March Tests to Processor Cache Memory Tags**
  Georgios A.THEODOROU, Nektarios KRANITIS, Antonis PASCHALIS, Univ. of Athens, Greece, Dimitris GIZOPOULOS, Univ. of Piraeus, Greece.
- **Analysis of Resistive-Bridging Defects in SRAM Core-Cell: Impact within the Core-Cell and in the Memory Array**
  Renan ALVES FONSECA, Alberto BOSIO, Luigi DILILLO, Patrick GIRARD, Serge PRAVOSSOUDOVITCH, Arnaud VIRAZEL, LIRMM, France, Nabil BADEREDDINE, Infineon Technologies, France
- **Forward-Looking Reverse Order Fault Simulation for n-Detection Test Sets**
  Irith POMERANZ, Purdue University, USA, Sudhakar REDDY, University of Iowa, USA
- **Design-for-Debug of Mixed Signal Cores**
  Nuno DIAS, Angelo MONTEIRO, IST/INESC-ID Portugal, Marcelino SANTOS, Gabriel SANTOS, IST/INESC-ID and SiliconGate, Portugal, J.Paulo TEIXEIRA, INESC-ID/IST, Portugal

## 11:30 – 13:00 Session 3A: **Internal Testing of Mixed-Signal Cores**

*Moderators*: Florence AZAIS, LIRMM, France, Salvador MIR, TIMA, France

* **Testing of High Resolution ADCs Using Lower Resolution DACs Via Iterative Transfer Function Estimation**
Sehun KOOK, V. NATARAJAN, Abhijit CHATTERJEE, Georgia Tech., USA, Shalabh GOYAL, Le JIN, National Semicond. Corp., USA

** **Digital Signature Generator for Mixed-Signal Testing**
Ricard SANAHUJA, Alvaro GóMEZ, Luz BALADO, Joan FIGUERAS, Univ. Pol. de Catalunya, Spain

** **Simulations and Experimental results of INL Testing of 16-b A/D Converters without Accurate Test Stimulus**
Esa KORHONEN, Juha KOSTAMOVAARA, University of Oulu, Finland

## 11:30 – 13:00 Session 3B: **Debug and Validation**

*Moderators*: Rob AITKEN, ARM, USA, Miron ABRAMOVICI, Dafca Corp., USA

* **Speed Path Debug Using At-Speed Scan Test Patterns**
Ruifeng GUO, Wu-Tung CHENG, Kun-Han TSAI, Mentor Graphics Corp, USA

* **Resource-Efficient Programmable Trigger Units for Post-Silicon Validation**
Ho Fai KO, Nicola NICOLICI, McMaster University, Canada

** **The Role of Mutation Analysis for Property Qualification**
Graziano PRAVADELLI, Franco FUMMI, Luigi DI GUGLIELMO, Università di Verona, Italy

## 11:30 – 13:00 Session 3C: **Vendor Session 1**

*Moderators*: Marcelino SANTOS, IST/INESC-ID, SiliconGate, Portugal, Regis LEVEUGLE, TIMA, France

**Advanced DFT Techniques for Deep Sub-micron Design**
Nikolaus MITTERMAIER, Synopsys, USA

**Emerging Standards for Digital Test and Diagnosis**
Geir EIDE, Mentor Graphics Corporation, USA

**The ARM Standardized MBIST Port**
Teresa MCLAURIN, ARM, USA

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## 13:00 – 14:30 LUNCH

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## 14:30 – 16:00 Session 4A: **Power Issues During Test**

*Moderators*: Sebastian SATTLER, Friedrich-Alexander Univ., Erlangen-Nürnberg, Germany, Patrick GIRARD, LIRMM, France

* **On Minimization of Peak Power for Scan Circuit during Test**
Jaynarayan TUDU, Indian Inst. of Science, Bangalore, India, Erik LARSSON, Linkoping Univ., Sweden, Virendra SINGH, Indian Inst. of Science, Bangalore, India, Vishwani AGRAWAL, Auburn University, USA

** **Understanding Power Issues during ATPG Using Volume Diagnosis**
Davide APPELLO, Vincenzo TANCORRE, Davide PANDINI, Roberto MATTIUZZO, Patrice DORIOL, STMicroelectronics, Italy, Salvatore TALLUTO, M. HALL, C. SUZOR, R. KAPUR, Synopsys, Inc., USA

** **Built-In Test Driven Power Aware Self Tuning of Wideband RF Devices**
Shyam Kumar DEVARAKOND, VISHWANATH NATARAJAN, Shreyas SEN, Abhijit CHATTERJEE, Georgia Inst. of Technology, USA

## 14:30 – 16:00 Session 4B: **Self-test and Test Throughput**

*Moderators*: Cecilia METRA, Univ. of Bologna, Italy, Gert JERVAN, Tallinn Univ., Estonia

* **Exploiting Thread-Level Parallelism in Functional Self-Testing of CMT Processors**
Andreas APOSTOLAKIS, Mihalis PSARAKIS, Dimitris GIZOPOULOS, Univ. of Piraeus, Greece, Antonis PASCHALIS, Univ. of Athens, Greece, Ishwar PARULKAR, Sun Microsystems, USA

* **Doubling Test Cell Throughput by On-Loadboard Hardware, Implementation and Experience in a Production Environment**
ANDREAS LEININGER, Frank-Uwe FABER, Matthias BECK, Markus RUDACK, Olivier BARONDEAU, Infineon Technologies AG, Germany, Thomas RABENALT, MICHAEL GOESSEL, University Potsdam, Germany

* **Algorithms for ADC Multi-Site Test with Digital Input Stimuli**
Xiaoqin SHENG, Hans KERKHOFF, Univ. of Twente, the Netherlands,
AMIR C ZJAJO, Guido GRONTHOUD, NXP Semiconductors, the Netherlands

## 14:30 – 16:00 Session 4C: **Vendor Session 2**

*Moderators*: Nicola NICOLICI, McMaster University, Canada, Zdenek KOTASEK, Brno University of Technology, Czech Republic

**Early Detection Solution Improves Profitability across Global Operations**

Debbora Ahlgren, OptimalTest, Israel

**Test Program Maintenance and Optimization**
Meir GELLIS, TestInsight, Ltd., Israel

**Effectiveness of an RTL Design for Test Solution on an Industrial Test Case**
Chouki AKTOUF, Ivano MIDULLA, DeFacto Technologies, France

## 16:00 – 17:00 Session 5: **Poster Session II**

- **A Low-Cost on-chip Design Platform for static ADC Measurements**
  Brendan MULLANE, C MACNAMEE, Vincent O BRIEN, Thomas FLEISCHMANN, Univ. of Limerick, Ireland
- **Early Pruning of Soft Errors and Transient Faults with Petri Nets**
  Paolo MAISTRI, Regis LEVEUGLE, TIMA Lab., France
- **An Efficient Approach to the Generation of Test Programs for Cache Controller**
  Wilson-Javier PEREZ HOLGUIN, Universidad del Valle, Colombia, Danilo RAVOTTO, Ernesto SANCHEZ, Matteo SONZA REORDA, Politécnico di Torino, Italy
- **Test Generation and DFT Based on Partial Thru Testability**
  Nobuya OKA, Hiroshima City University, Japan, CHIA YEE OOI, Universiti Teknologi Malaysia, Malaysia, Hideyuki ICHIHARA, Tomoo INOUE, Hiroshima City University, Japan, Hideo FUJIWARA, Nara Institute of Science and Technology (NAIST), Japan
- **Simulation Methodology for the Validation of Low Energy Particle Accelerators as Fault Injection Tools**
  Juan M. MOGOLLÓN, Rogelio PALOMO PINTO, Miguel A. AGUIRRE, Javier NÁPOLES, Hipólito GUZMÁN-MIRANDA, Univ. of Sevilla, Spain
- **BISR Architecture and Methodology for Fault-Tolerant Embedded Memories**
  Nicholas AXELOS, Kiamal Z PEKMESTZI, National Technical University of Athens, Greece
- **Towards an Integrated Environment to Enhance Yield Learning**
  Simona PAPPALARDO, ST Microelectronics, Italy
- **Dynamic Interconnect Testing in Multi-Bus, Multi-FPGA Digital Systems**
  Carlos LEONG, Vasco BEXIGA, Pedro MACHADO, Isabel TEIXEIRA, João Paulo TEIXEIRA, INESC-ID/IST, Portugal
- **System-Level Hardware-Based Protection Scheme against Memory Errors**
  Valentin GHERMAN, Samuel EVAIN, Mickaël CARTRON, Yannick BONHOMME, CEA, LIST, France

## 17:00 – 18:00 Session 6A: **On-line Testing**

*Moderators*: Marie-Lise FLOTTES, LIRMM, France, Salvador BRACHO, Univ. of Cantabria, Spain

* **Concurrent Self-Test with Partially Specified Patterns for Low Test Latency and Overhead**
Michael KOCHTE, Christian ZOELLIN, Hans-Joachim WUNDERLICH, Univ. of Stuttgart, Germany

** **Low Cost On-Line Testing of the Schedule of High Performance Microprocessors**
Cecilia METRA, Daniele ROSSI, Martin Eugenio OMANA, Univ. of Bologna, Italy, Abhijit JAS, Rajesh GALIVANCHE, Intel Corp., USA

## 17:00 – 18:00 Session 6B: **Vendor Session 3**

*Moderators*: Erik LARSON, Linkoping Univ., Sweden, Matteo SONZA-REORDA, Polit. Torino, Italy

**Single Event Affects a Test Strategy for New Technologies and Nowadays Needs**
Gonzalo FERNÁNDEZ, ALTER Technology Group, Spain

**Evaluation of Optoelectronic Components for Space Applications**
Juan BARBERO, Enrique CORDERO, Laura PEÑATE, Alina SPUMA, Javier PÉREZ, Sara DIAZ, ALTER Technology Group, Spain

## 18:00 – 19:30 Session 7A: **Panel 1**

*Organizers:* Said HAMDIOUI, TU Delft, the Netherlands, Simona PAPPALARDO, ST Microelectronics, Italy
*Moderator*: Tom W. WILLIAMS – Synopsys, USA

**Yield, Reliability, and Variability in the Nano-Era: Will Existing Approaches Survive?**

Panelists: Debbora Ahlgren – OptimalTest, Israel
Brady Benware – Mentor Graphics, USA
Teresa McLaurin – ARM, USA
Udo Schwalke – Techn. University Darmstadt, Germany
Srikanth Venkataraman – Intel, USA

Abstract: It is widely recognized that variability in device characteristics and the new failure mechanisms in the nano-technology era will severely impact the design, manufacturing, and testing of future chips. In addition, time-to-market and time-to-volume pressure have created major engineering challenges in rapid yield learning and guaranteeing the required quality and reliability.

The panel aims at gathering opinions on the different ways to deal with these challenges in order to survive the nano-era. Can we still rely on test data analysis to accurately predict the reliability of the manufactured chips? Can today's methodologies such as burn-in still be able to provide the required reliability? Can statistics provide the necessary information of the root cause of yield loss without performing the time-consuming physical failure analysis? Are existing test approaches still able to deliver the required product quality even if the failure mechanisms are shifting from permanent faults to intermittent and transient faults? Does the impact on memory differ from the impact on logic?

## 18:00 – 19:30 Session 7B: **Panel 2**

*Organizer and Moderator*: Hans-Joachim WUNDERLICH, Universität Stuttgart, Germany

**Extended Diagnosis Requirements in Automotive Applications**

*Panelists:* Davide Appello, STM, Italy
Stephen Sunter, LogivVison, USA
Frank Poehl, Infineon, Germany
Sebastian Sattler, Germany

Abstract: The cars of today show more and more functions and features implemented in hardware and software which were formerly realized by mechanics. In addition, a tremendous amount of new functionalities are added like automatic distance holding, road recognition or the complete infotainment which require a computing power formerly only seen in super computers. As a consequence, the gap between very mature technology for car microelectronics and most advanced technology for high performance computing is reduced year by year, and debug and diagnosis are now also severe challenges for the automotive industry.

Time consuming diagnosis procedures where car makers and different suppliers are involved may cause tremendous costs for delayed production or delivery, call for returns or repair. The session will discuss how design for test, embedded diagnosis or testability considerations and features at the ASIC level can help at system level.

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# Wednesday, May 27, 2009

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## 9:00 – 10:30 Session 8A: **Advanced Testing of Memories, Power Transistors and Microfluidic Systems**

*Moderators*: Ondřej NOVÁK, Czech Technical Univ., Czech Republic, Krish CHAKRABARTY, Duke Univ., USA

* **Design and Test Challenges in Resistive Switching RAM (ReRAM): An Electrical Model for Defect Injections**
Olivier GINEZ, Jean Michel PORTAL, Christophe MULLER, Univ. de Provence (Aix-Marseille I), France

* **Novel Solution for the Built-in Gate Oxide Stress Test of LDMOS in Integrated Circuits for Automotive Applications**
Vezio MALANDRUCCOLO, Mauro CIAPPA, Wolfgang FICHTNER, Swiss Federal Inst. of Technology (ETH), Switzerland, Hubert ROTHLEITNER, Infineon Technologies, Austria

* **Built-in Test Solutions for the Electrode Structures in Bio-Fluidic Microsystems**
Quis AL-GAYEM, Hongyuan LIU, Andrew RICHARDSON, Lancaster University, UK

## 9:00 – 10:30 Session 8B: **Recent Advances in ATPG**

*Moderators*: Zebo PENG, Linkoping Univ., Sweden, Nicola BOMBIERI, Univ. of Verona, Italy

* **Increasing Robustness of SAT-based Delay Test Generation using Efficient Dynamic Learning Techniques**
Stephan EGGERSGLUESS, Rolf DRECHSLER, University of Bremen, Germany

* **Input Cubes with Lingering Synchronization Effects and their Use in Random Sequential Test Generation**
Irith POMERANZ, Purdue University, USA, Sudhakar REDDY, University of Iowa, USA

* **Automatic Functional Stress Pattern Generation for SoC Reliability Characterization**
Paolo BERNARDI, Matteo SONZA REORDA, Michelangelo GROSSO, Ernesto SANCHEZ, Politecnico di Torino, Italy, R. CAGLIESI, M. GIANCARLINI, ELES Semiconductor Equipment, Italy, Davide APPELLO, STMicroelectronics, Italy

## 9:00 – 10:30 Session 8C: **Student's Forum**

*Moderators*: John HAYES, Univ. of Michigan, USA, Ilia POLIAN, Freiburg Univ., Germany

- **Resistive Bridging Faults - Defect-Oriented Modeling and Efficient Testing**
  Piet ENGELKE, Albert-Ludwigs-University, Freiburg, Germany
- **Power-Supply and Temperature Based Methodologies to Improve Tolerance and Detection of Delay Faults in Synchronous Digital Circuits**
  Jorge SEMIÃO, INESC-ID/IST, Univ. Algarve, Portugal
- **Improving SAT-based ATPG**
  Alejandro CZUTRO, Albert-Ludwigs-University, Freiburg, Germany
- **Advanced Techniques for Automatic Test Pattern Generation using Boolean Satisfiability**
  Daniel TILLE, University of Bremen, Germany
- **Fault Tolerance Architecture for Reliable Hybrid CMOS/Nanodevices Memory**
  Nor Zaidi HARON, Zaiyan AHYADI, Delft University of Technology, The Netherlands
- **Current Monitoring of Power Structures Using Magnetic Force Sensor**
  Martin DONOVAL, Martin DAŘíČEK, Juraj MAREK, Slovak University of Technology, Slovakia
- **SoC Yield Improvement for Future Nanoscale Technologies**
  Julien VIAL, LIRMM, France
- **Testing of Delay Faults in Asynchronous Circuits**

Roland DOBAI, Slovak Academy of Sciences, Slovakia

- **Performance/hardware overhead estimation of ADC BIST implementations**
  Peter MRAK, Jozef Stefan Institute, Ljubljana, Slovenia

- **A Mixed HDL/PLI Test Package**
  Nastaran NEMAT, University of Tehran, Iran

- **A Logic Diagnosis Approach for Sequential Circuits**
  Youssef BENABBOUD, LIRMM, France

- **Test Pattern Generation and Compaction for Crosstalk Induced Glitch Faults**
  Shehzad HASAN, University of Bremen, Germany

## 10:30 – 11:30 Session 9: **Student's Posters**

## 11:30 – 13:00 Session 10A: **Advanced External Testing of Mixed-Signal Cores**

*Moderators*: Einar AAS, Norway University of Science, Norway, Luz BALADO, Univ. Pol. de Catalunya, Spain

* **Defect Filter for Alternate RF Test**
Haralampos STRATIGOPOULOS, Salvador MIR, TIMA Laboratory, France, Erkan ACAR, Duke University, USA, Sule OZEV, Arizona State University, USA

* **Signature-Based Testing for Digitally-Assisted Adaptive Equalizers in High-Speed Serial Links**
Mohamed ABBAS, University of Tokyo, Japan, Kwang-Ting (Tim) CHENG, Univ. of California, Santa Barbara, USA, Yasuo FURUKAWA, ADVANTEST Corp., Japan, Satoshi KOMATSU, Kunihiro ASADA, University of Tokyo, Japan

** **Optimization of a Structural DfT Targeting Fault Detection on High-Speed ADCs**
Yolanda LECHUGA, Roman MOZUELOS, Mar MARTINEZ, Salvador BRACHO, Universidad de Cantabria, Santander, Spain

## 11:30 – 13:00 Session 10B: **Diagnosis and Dependability Analysis**

*Moderators*: Peter HARROD, ARM, U.K., Alex BYSTROV, Newcastle Univ., UK

* **A Two Phase Approach for Minimal Diagnostic Test Set Generation**
Mohammed SHUKOOR, Vishwani AGRAWAL, Auburn University, USA

* **Categorizing and Analysis of Activated Faults in the FlexRay Communication Controller Registers**
YASSER SEDAGHAT, Seyed Ghassem MIREMADI, Sharif University of Technology, Tehran, Iran

** **Improving Diagnostic Test Generation for Scan Chain Failures Using Sequential Patterns**
Xun TANG, Univ. of Iowa, Ruifeng GUO, Wu-Tung CHENG, Mentor Graphics Corp., Sudhakar REDDY, Univ. of Iowa, Yu HUANG, Mentor Graphics Corp., USA

## 11:30 – 12:30 Session 10C: **Special Session on Soft Errors in Electronic Systems**

*Moderators*: Sybille HELLEBRAND, Univ. of Paderborn, Germany, Raoul VELAZCO, TIMA, France

(153) [SS] **Complex Electronic Systems Soft Error Rate (SER) Management**
Dan Alexandrescu, Iroc, France, Shi-Jie Wen, Cisco, USA, Michel Nicolaidis, TIMA Lab., France

Abstract : This talk describes recent breakthroughs on Single Event Effects analysis techniques for complex ASICs and SoCs. We propose a systematic method for the evaluation of the system Soft Error

Rate (SER) based on reliability-like, higher-level SER budgeting and hierarchical breakdown of SER constraints through all the levels of the design flow from the system architecture to the final chip implementation. The approach is particularly adapted for evaluating the SER of difficult-to-tackle sophisticated SoCs, such as networking chips, whose designers are confronted today with increasingly demanding reliability requirements. Practical mitigation solutions guided from the analysis results are also addressed.

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## 13:00 – 14:30 LUNCH

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## 14:30 – 15:30 Session 11A: **Embedded Tutorial 1**

*Moderator*: Bernd BECKER, Freiburg University, Germany

### Switching Noise and Process Variability Challenges in Delay Testing

Adit SINGH, Auburn University, USA

Abstract : Delay defects that degrade performance and cause reliability failures are emerging as a major problem in nanometer technologies. Small delay defects represent a significant reliability concern when resistive defects are present in a technology. A low level of resistive defects can be overcome with typical TDF testing, however when the defect rate increases, traditional TDF testing is insufficient to achieve low DPPM levels. Today, additional stresses are necessary to age these defects to the point where TDF tests can screen them. In order to achieve low DPPM levels without additional acceleration such as burn-in, fine delay defect screening appears to offer a solution. Structural scan based delay testing is being actively pursued as a possible solution. However, recent research indicates that several formidable challenges must be overcome before it can become fully effective. A major limitation of scan timing tests is that they operate the circuit outside of the normal functional mode. The single fast launch-to-capture clock period in the scan test is assumed to provide a single cycle snapshot of circuit timing observed in uninterrupted normal functional operation. Signal delays in this clock window are checked and verified against the desired clock rate. Unfortunately, this observed signal timing may not reflect true circuit delays in normal functional operation for several reasons. (1) Power supply noise (IR drops) from abnormal excessive switching activity from scan vectors. (2) Activation of multi-cycle paths and false paths. (3) Excessive coupling noise and crosstalk effects due to non-functional switching patterns. (4) Device performance variation due to a different die temperature profile during test as compared to functional operation. (5) “Clock stretching” -the inability of the clock tree to reach timing stability for a single fast capture clock pulse. It is to avoid unacceptable yield loss from false failure indications (“over testing”) due to these timing uncertainties that force scan delay tests to be often run slower than rated speed, limiting their effectiveness. Detection of small delay defects by scan tests is further compromised by additional factors that also impact functional timing tests: (6) Timing margins required to allow for the increasing variations in process parameters. (7) Short paths that can absorb many small delay defects within the circuit timing slacks.

The proposed tutorial will explain and illustrate these test challenges. State-of-the-art test methodologies aimed at overcoming these challenges are presented, and their effectiveness and limitations discussed, based on published experimental studies. These include using only functionally validated LOC test vectors to mimic (one-cycle) functional operation during the scan test thereby avoiding abnormal circuit activity and activation of false paths; multi-cycle capture to minimize clock stretching as supported by EDA test tools; Cadence’s Tru-Time based faster-than-rated-clock test methodology to target small delay defects on short paths; and Scan delay test based speed binning studies from Nvidia and Freescale. Promising new research ideas not yet adopted by industry, such as comparison timing testing of multi-core processors, will also be discussed.

## 14:30 – 15:30 Session 11B: **Embedded Tutorial 2**

*Moderator*: Yervant ZORIAN, VirageLogic, USA

### Test Challenges and Solutions in TSV-Based 3D Stacked ICs

Krishnendu CHAKRABARTY, Duke University, USA, Erik Jan MARINISSEN, IMEC, Belgium

Abstract : In the continuing quest for high-density high-performance low-power integrated circuits, new developments in processing technology now start to allow us to stack multiple integrated circuits on top of each other, interconnected by many Through-Silicon Vias (TSVs). This next step in the sequence flip-

chip, Multi-Chip Module, and System-In-Package, has multiple attractive benefits: (1) Heterogeneous integration: each die can be made in a dedicated technology, for example optimized for digital logic, memory, analog, RF, sensors, etc.; (2) Higher yield, if one large die is divided over multiple smaller dies; (3) Small footprint, as multiple dies are stacked vertically on top of each other; (4) Small volume, as dies are thinned and stacked with very little space in between; (5) High performance, as TSVs allow much faster and wider communication paths between dies than traditional wires; and (6) Low power, as TSVs have much less capacity than traditional wires.

While architects, designers, and EDA folks are preparing to take advantage of the new third dimension in chip design, test solutions should follow suit in order to make this technology industrially viable.

This embedded tutorial gives an overview of the field and highlights the corresponding test challenges and emerging test solutions. It targets both industrial engineers, who want to be prepared for what is ahead, as well as researchers that hope to contribute to this hot and exciting domain.

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16:00 – 23:00 SOCIAL PROGRAM

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## Thursday, May 28, 2009

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### 9:00 – 10:30 Session 12A: **Impact of Nanometer Technologies in the Testing Methodology**

*Moderators*: Michel RENOVELL, LIRMM, France, Salvador MANICH, Univ. Pol. de Catalunya, Spain

* **Low-Complex Off-Chip Skew Measurement and Compensation Module (SMCM) Design for Built-Off Test Chip**
Kihyuk HAN, Joonsung PARK, Jae Wook LEE, Jacob ABRAHAM, the Univ. of Texas at Austin, USA, Eonjo BYUN, Cheol-Jong WOO, Sejang OH, Samsung Electronics, Korea

** **New Repeatability & Reproducibility Methodology for Semiconductor Testing**
Sergio TENUCCI, Marco SPINETTA, Alberto PAGANI, Bernard RANCHOUX, STMicroelectronics, Italy and France

* **A voltage-mode testing method to detect IDDQ defects in digital circuits**
Josep RIUS, Univ. Pol. Catalunya, Spain, Luis ELVIRA, Maurice MEIJER, NXP Semiconductors, the Netherlands

### 9:00 – 10:30 Session 12B: **DfT and Embedded Test**

*Moderators*: Jerzy TYSZER, Poznan Univ. of Technology, Poland, Andreas GLOWATZ, Mentor Graphics Hamburg, Germany

* **Partial Scan Approach for Secret Information Encoding**
MICHIKO INOUE, Tomokazu YONEDA, Muneo HASEGAWA, Hideo FUJIWARA, Nara Institute of Science and Technology (NAIST), Japan

* **Masking of X-values by use of a hierarchically configurable register**
Thomas RABENALT, Univ. of Potsdam, Andreas LEININGER, Infineon Technologies AG, Michael GOESSEL, Univ. of Potsdam, Germany

* **Test Encoding for Extreme Response Compaction**
Stefan HOLST, Michael KOCHTE, Melanie ELM, Hans-Joachim WUNDERLICH, Univ. of Stuttgart,

Germany

## 10:30 – 11:30 Session 13: **Poster Session III**

- **Memory Test and Diagnosis using Automated Pattern Generation**
  Joerg VOLLRATH, Qimonda AG, Germany
- **Test Data Reduction by Test Point Insertion Based on Necessary Assignment**
  Kazuko HIRAMOTO, Yuki YOSHIKAWA, Hideyuki ICHIHARA, Tomoo INOUE, Hiroshima City University, Japan
- **Start-Up of a Pulsed Laser Test System for Single Event Effects Analysis**
  Fco. Rogelio PALOMO PINTO, Juan MOGOLLÓN, Javier NÁPOLES, Hipólito GUZMÁN MIRANDA, José RODRíGUEZ, Alfredo VEGA-LEAL, Miguel AGUIRRE, J TOMBS, Univ. of Sevilla, C MÉNDEZ, J. R. VÁZQUEZ DE ALDANA, P. MORENO, Univ. of Salamanca, L. ROSO, Centro de Láseres Pulsados Ultracortos Ultraintensos (CLPU). Salamanca, Spain
- **Improving Soft Error Correction Capability of 4-D Parity Codes**
  Zaid AL-ARS, Muhammad IMRAN, Georgi GAYDADJIEV, Delft University of Technology, The Netherlands
- **Handling More X's Using Current X-Tolerant Compactors with Maximal Compaction**
  YOUHUA SHI, Nozomu TOGAWA, Masao YANAGISAWA, Tatsuo OHTSUKI, Waseda University, Japan
- **A Black-Box Software-Based Self-Test for Embedded Microprocessors**
  Stefano DI CARLO, Paolo PRINETTO, Gianfranco POLITANO, Alessandro SAVINO, Politecnico di Torino, Italy
- **Fast BER Test for Digital RF Transceivers**
  Jerzy DABROWSKI, Linkoping Univ., Sweden
- **A BiST Jitter Characterization Solution for use with Low Cost Automatic Test Equipment**
  Jacob ABRAHAM, Sachin DASNURKAR, The Univ. of Texas at Austin, USA

## 11:30 – 12:30 Session 14A: **Embedded Tutorial 3**

*Moderator*: Adelio SALSANO, University of Roma II, Italy

**Ensuring High Testability without Degrading Security**
Giorgio di NATALE, Marie-Lise FLOTTES, Bruno ROUZEYRE, LIRMM, France, Paolo MAISTRI, Regis LEVEUGLE, TIMA Lab., France

Abstract : Cryptographic algorithms are used to protect sensitive information from untrusted parties when the communication medium is not secure. Many secure systems such as smartcards include hardware implementation of symmetric cryptographic algorithms such as (Triple) Data Encryption Standard and Advanced Encryption Standard. The secret keys used to encrypt the data with these algorithms are large enough to prevent any brute force attack that consists in exploring the whole solution space. However, the hardware implementation of these cryptographic algorithms allows the hackers to measure the observable characteristics of the physical implementation and deduce the secret key (side-channel attacks). The key can even be discovered by applying a side-channel attack on scan chains. These scan chains, which aim to provide full controllability and observability of internal states, represent nevertheless the most popular design-for-testability scheme. Because crypto-processors and others cores in a secure system must pass through high-quality test procedures to ensure that data are correctly processed, testing of crypto chips faces a dilemma: how to develop a design-for-testability scheme that provides high testability (high controllability and observability) while maintaining high security (minimal controllability and observability)? This tutorial presents the security weaknesses generated by scan designs on hardware AES and DES implementations. It also discusses the pros and cons of security-dedicated DFT, BIST and Fault tolerance solutions taken from the literature.

## 11:30 – 12:30 Session 14B: **Embedded Tutorial 4**

*Moderator*: Hans KERKHOFF, Univ. Twente, The Netherlands

**On-chip Delay Measurement Techniques for Production Test – from Digital to Analog**
Stephen SUNTER, LogicVision, USA

Abstract : As CMOS IC dimensions scale below 90 nm, delays-of-interest range from nanoseconds to picoseconds. Greater time measurement accuracy is needed but off-chip delay measurement techniques are becoming severely limited by fundamental properties of signal access paths off-chip and on-chip, such as noise, wire length, and impedance variation. On-chip measurement techniques have been proposed by IC designers, DFT engineers, and test engineers, with claimed accuracies ranging from nanoseconds to femtoseconds, at least in simulation.

This embedded tutorial will survey most of the papers that provide silicon results published in the last 10 years, in both design and test journals/conferences, and some representative papers that include only simulated results, to discover the most promising directions for measuring and production testing today's and future delays-of-interest. Delay parameters include instantaneous delay, average delay, and delay variation (long and short term, including jitter) in digital and analog paths, which inevitably depend on voltage, frequency, and temperature. The measurement techniques will be categorized by suitability for measurement of one-shot and periodic events, then by measurement principle, and lastly by circuit technique and reported real-silicon capabilities. The goal is to identify principles and general techniques suitable for production testing of digital and perhaps analog circuitry, which means high resolution, wide range, quick test time, process tolerance, and insignificant silicon area.

12:30 – 13:00 **Closing Session**

12:30 – 12:45 **Closing Remarks**
Jose Luis Huertas, CNM, Spain – ETS'09 General Chair

12:45 – 13:00 **Introduction to ETS'10**
Ondrej Novak, Czech Technical Univ., Czech Republic, ETS'10 General Chair

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13:00 – 14:30 LUNCH

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## Friday, May 29, 2009

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## ETS'09 Fringe Workshop

9:00 – 13:00 and 14:30 – 17:30

**LPonTR'09**

**Impact of Low-Power design on Test and Reliability**